TPS728185315EVM-267

This user's guide describes the characteristics, operation, and use of the TPS728185315EVM-267 evaluation module (EVM). This EVM contains two TPS728185315 low-dropout linear regulator ICs, one in the chipscale (YZU) package and the other in the 2mmx2mm QFN (DRV) package. This document includes EVM specifications, recommended test setup, test results, bill of materials (BOM), and a schematic diagram.

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1 Introduction

The Texas Instruments TPS728185315EVM-267 evaluation module contains two TPS728185315 low-dropout linear regulator ICs, one in the chipscale package (YZU) and the other in the 2 mm × 2 mm QFN (DRV) package. The TPS728185315 can provide up to 200 mA of dc current and the output voltage can be quickly switched between 1.85 V and 3.15 V using the VSET pin. The goal of the EVM is to facilitate evaluation of the TPS728185315 IC.

1.1 Performance Specification Summary

Table 1 provides a summary of the TPS728185315EVM performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Typical Performance Specification Summary

	CONDITION	VOLTAGE RANGE (V)			CURRENT RANGE (mA)		
		MIN	TYP	MAX	MIN	TYP	MAX
V_{BIAS} IN	V_O = 1.85 V	2.7		6.5 (1)		200	
V_{IN} IN	V_O = 3.15 V	3.55		6.5 (1)		200	
V_{OUT}		1.795	1.85	1.906			200 (1)
V_{OUT}		3.056	3.15	3.245			200 (1)

(1) Linear regulator power dissipation is computed as $P_D = (V_{IN} – V_{OUT}) \times I_{OUT}$. As specified in the data sheet, the regulator's package has a finite power dissipation rating depending on the ambient temperature, board type, and airflow. Using V_{IN} and/or V_{OUT} voltages other than the typical voltages recommended in the table or using the EVM in an environment with an ambient temperature higher than 25°C significantly reduces the maximum allowed output current. See the data sheet for the regulator package's thermal resistance data, and see TI application report *Digital Designer's Guide to Linear Voltage Regulators and Thermal Management* (SLVA118) for a full explanation.

1.2 Modifications

To aid user customization of the EVM, the board was designed with devices having 0603 or larger footprints. A real implementation likely occupies less total board space.

Changing components can improve or degrade EVM performance. For example, adding a larger output capacitor reduces output voltage undershoot but lengthens response time after a load transient event. Adding a larger input capacitor reduces droop at the V_{IN} pin that inductive leads from the V_{IN} power supply may cause during a load transient.

2 Input/Output Connector Descriptions

J1–VIN Positive connection to the power input supply (V_{IN}) for the QFN (DRV) packaged IC.

J2–VOUT Positive connection for the output load on V_{OUT} for the QFN (DRV) packaged IC.

J3–GND Return connection for the input supply for both ICs.

J4–GND Ground return connection for the output load for both ICs.

J5–VIN Positive connection to the power input supply (V_{IN}) for the chipscale (YZU) packaged IC.

J6–VOUT Positive connection for the output load on V_{OUT} for the chipscale (YZU) packaged IC.

JP1– ON/EN/OFF - When this jumper is placed in the ON position, the chipscale (YZU) device's ENable pin is tied to V_{IN}, thereby enabling the device. When the jumper is placed in the OFF position, the the chipscale (YZU) device's ENable pin is tied to ground, thereby disabling the device.

JP2– VOUT2/VSET/VOUT1 - When this jumper is placed in the VOUT2 position, the QFN (DRV) packaged device's VSET pin is tied to V_{IN}, thereby setting V_{OUT} = 3.15 V. When the jumper is placed in the VOUT1 position, the the QFN (DRV) packaged device's VSET pin is tied to ground, thereby setting V_{OUT}=1.85 V.

JP3– VOUT2/VSET/VOUT1 - When this jumper is placed in the VOUT2 position, the chipscale (YZU) packaged device's VSET pin is tied to V_{IN}, thereby setting V_{OUT} = 3.15 V. When the jumper is placed in the VOUT1 position, the the chipscale (YZU) packaged device's VSET pin is tied to ground, thereby setting V_{OUT}=1.85 V.

JP4– ON/EN/OFF - When this jumper is placed in the ON position, the QFN (DRV) device's ENable pin is tied to V_{IN}, thereby enabling the device. When the jumper is placed in the OFF position, the QFN (DRV) device's ENable pin is tied to ground, thereby disabling the device.

TP1 – Test point for measuring V_{IN} for the QFN (DRV) packaged device.

TP2 – Test point for measuring V_{OUT} for the QFN (DRV) packaged device.

TP3 – Test point for measuring board ground.

TP4 – Test point for measuring V_{IN} for the chipscale (YZU) packaged device.

TP5 – Test point for measuring V_{OUT} for the chipscale (YZU) packaged device.

2.1 Test Setup

The maximum recommended voltage allowed on the IN terminal is 6.5V with the maximum on EN or VSET being V_{IN}. Headers J1 and J5 are not connected. So, connect the positive side of separate or one input power supply to headers J1 and J5 and the negative (ground) side header J3. To enable the QFN (DRV) packaged regulator, place JP1 in the ON postion. To enable the chipscale (YZU) packaged regulator, place JP4 in the ON postion. Use JP2 or JP3 to change the output voltage of the DRV and YZU packages respectively, between VOUT1 =1.85V and VOUT2 = 3.15V. When connecting the positive side of external loads to either header J2 or J6 and the negative (ground) side to header J4, use short, twisted leads in order to minimize DC drop at the connector and/or inductive voltage dip after a transient load is removed. Additional input capacitance may be required if the input power supply is connected to the boards via long leads and/or fast load transients are applied to the output.

2.2 Test Results

Figure 1 shows the test results at T_A = 25°C using this EVM:

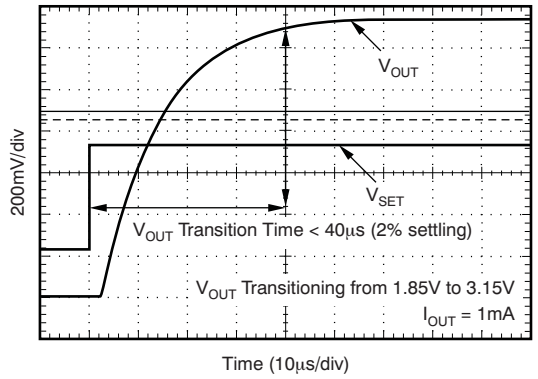

Figure 1. VSET Toggled Low to High, I_{OUT} = 1 mA

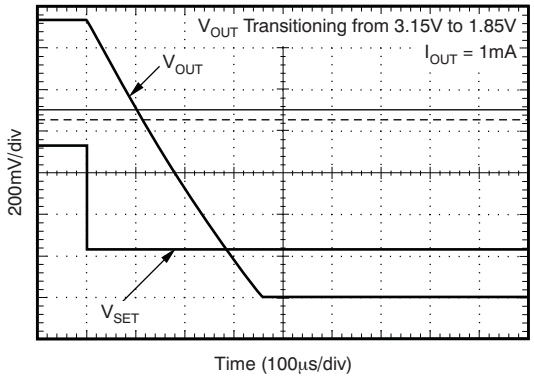

Figure 2. VSET Toggled High to Low, I_{OUT} = 1 mA

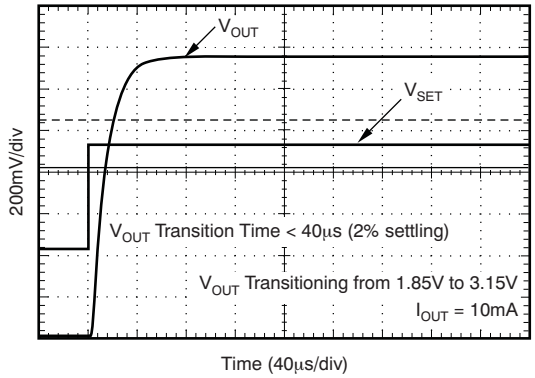

Figure 3. VSET Toggled Low to High, I_{OUT} = 10 mA

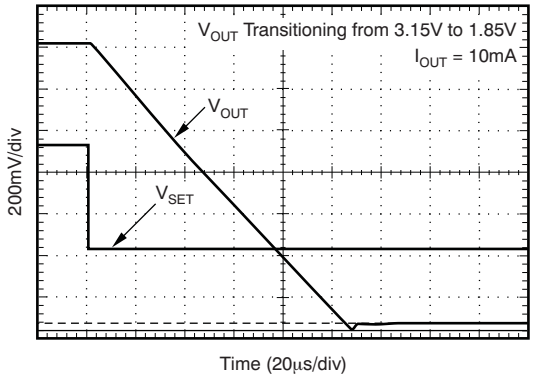

Figure 4. VSET Toggled High to Low, I_{OUT} = 10 mA

3 Board Layout

Board layout is important for best PSR and lowest noise. Figure 5, Figure 6, and Figure 7 show the board layout for the HPA267 PWB. See the data sheet for more specific layout guidelines.

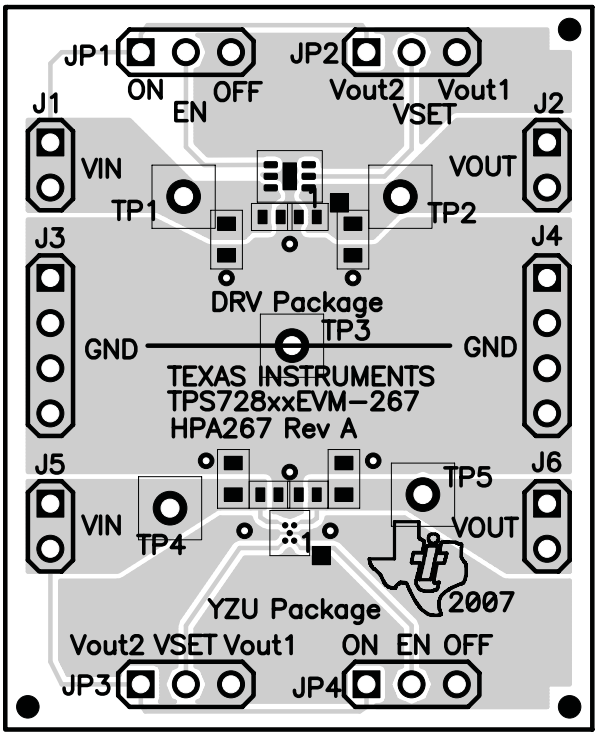

Figure 5. Top Assembly Layer

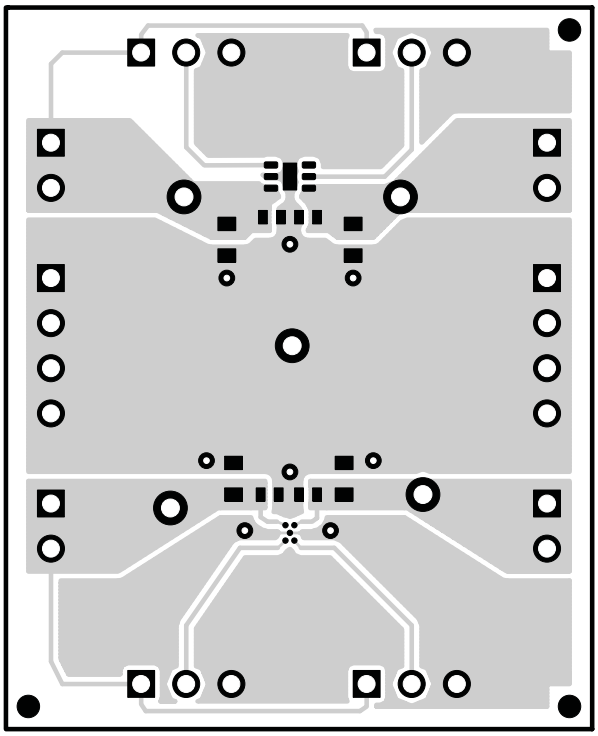

Figure 6. Top Layer

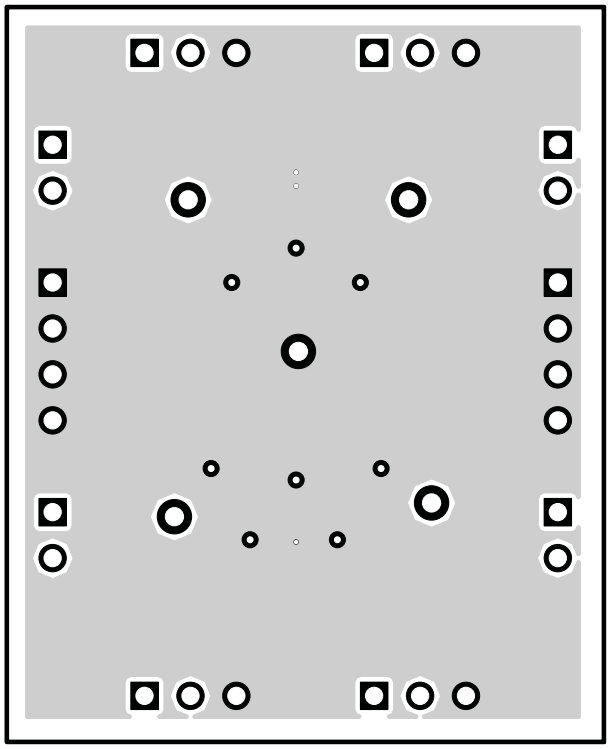

Figure 7. Bottom Layer

4 Bill of Materials and Schematic

4.1 Bill of Materials

Table 2. HPA267 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
0	C1, C4, C5, C8	Open	Capacitor, Ceramic	0603		
2	C2, C3	1.0 µF	Capacitor, Ceramic, 10V, X5R, ±20%	0402	ECJ-0EB1A105M	Panasonic
2	C6, C7	1.0 µF	Capacitor, Ceramic, 10V, X5R, ±20%	0402	ECJ-0EB1A105M	Panasonic
2	J1, J2		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
2	J5, J6		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
2	J3, J4		Header, Male 4 pin, 100mil spacing, (36-pin strip)	0.100 × 4	PTC36SAAN	Sullins
2	JP1, JP2		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins
2	JP3, JP4		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins
2	TP1, TP2		Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100	5000	Keystone
2	TP4, TP5		Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100	5000	Keystone
1	TP3		Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100	5001	Keystone
1	U1		IC, 200 mA, LDO with Pin Selectable Dual Output Voltage Levels	SON-6	TPS728185135DRV	TI
1	U2		IC, 200 mA, LDO with Pin Selectable Dual Output Voltage Levels	WCSP	TPS728185315YZU	TI
1	—		PCB, 1.6 In × 1.3 In × 0.062 In		HPA267	Any
4	—		Shunt, 100mil, Black	0.100	929950-00	3M

4.2 Schematic Drawing

Figure 8 is the schematic for the TPS728185315EVM-267.

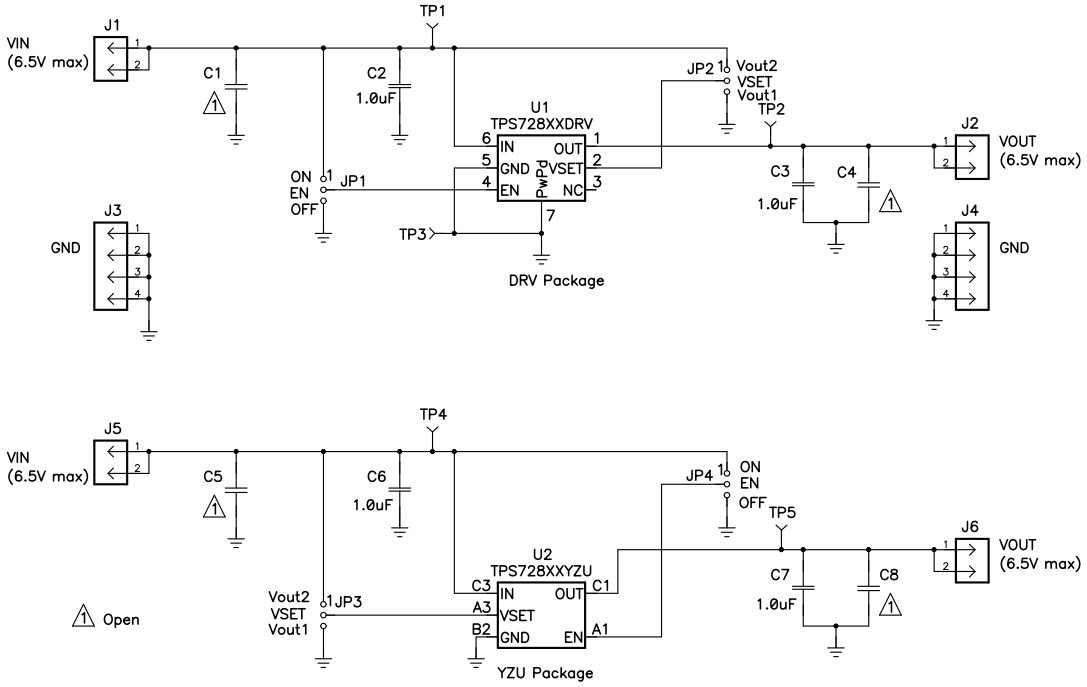

Figure 8. Schematic

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3 V to 5 V and the output voltage range of 3 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 25°C. The EVM is designed to operate properly with certain components above 25°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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